`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/12/2022 10:13:20 AM

// Design Name:

// Module Name: eightbit\_palu

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module eightbit\_palu(

input [7:0]a,

input [7:0]b,

input [1:0]s,

output reg [7:0]f,

output reg ovf

);

always @(s or a or b)

begin

case(s)

2'd0: //addition

begin

f = a+b;

ovf = (!a[7]&!b[7]&f[7]) + (a[7]&b[7]&!f[7]);

end

2'd1: //inv

begin

f = !b;

ovf = 0;

end

2'd2: //and

begin

f = a\*b;

ovf = 0;

end

2'd3: //or

begin

f = a|b;

ovf = 0;

End

default:

begin

f = a+b;

ovf = (!a[7]&!b[7]&f[7]) + (a[7]&b[7]&!f[7]);

end

endcase

end

endmodule